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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/750,532	12/30/2003	Chakki Kavoori	04303/100N160-US2	5596

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DARBY & DARBY P.C.
P.O. BOX 5257
NEW YORK, NY 10150-5257

EXAMINER	
ALI, SYED J	

ART UNIT	PAPER NUMBER
2195	

DATE MAILED: 06/10/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/750,532	KAVOORI ET AL.	
	Examiner	Art Unit	
	Syed J. Ali	2195	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 December 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 December 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *Dec. 30, 2003*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-20 are pending in this application.

Specification

2. The cross reference related to the application cited in the specification must be updated (i.e. update the relevant status, with PTO serial numbers or patent numbers where appropriate, on page 1, lines 8-9). The entire specification should be so revised.

3. An application in which the benefits of an earlier application are desired must contain a specific reference to the prior application in the first sentence of the specification or in an application data sheet by identifying the prior application by application number (37 CFR 1.78(a)(2) and (a)(5)). If the prior application is a non-provisional application, the specific reference must also include the relationship (i.e., continuation, divisional, or continuation-in-part) between the applications except when the reference is to a prior application of a CPA assigned the same application number.

Claim Objections

4. **Claims 2, 4, 10, and 17-18 are objected to because of the following informalities:**

a. In line 1 of each of claims 2, 4, 10, and 18, "apparatus" is misspelled as "appartatus".

b. In line 3 of claim 17, "mapping" is misspelled as "mapsping".

Appropriate correction is required.

Double Patenting

5. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Thorington,* 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

6. **Claims 1-2, 5, 9-10, and 14 are provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1 and 10-14 of copending Application No. 09/927,906.**

7. Although the conflicting claims are not identical, they are not patentably distinct from each other because they are both directed to traversing a linked list of hardware resources. Despite a slight difference in wording, the claims cover the exact same method steps.

This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

Claim Rejections - 35 USC § 101

8. 35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

9. **Claims 2, 4, 10-14, and 18-20 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter.**

10. As per claims 2, 4, 10, and 18, the claimed apparatus is at best a software apparatus, per se, failing to be tangibly embodied or including any recited hardware as part of the apparatus. Claims 11-14 and 19-20 are non-statutory for at least the same reasons as discussed for their parent claims, as they fail to present any limitations that resolve the deficiencies of their respective parent claims.

Claim Rejections - 35 USC § 102

11. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

12. **Claims 3-4 and 15-20 are rejected under 35 U.S.C. 102(e) as being anticipated by Kodosky et al. (USPN 6,608,638) (hereinafter Kodosky).**

13. As per claim 3, Kodosky teaches the invention as claimed, including in an electronic device having a processor, a memory, and at least one hardware resource coupled to each other, a method of dynamically implementing changes for scheduling the at least one hardware resource, the method comprising the steps of:

a) receiving a first list of addresses associated with the at least one hardware resource, the first list of addresses listing active operation information for the at least one hardware resource (col. 31 lines 36-38; col. 31 line 54 - col. 32 line 55);

b) receiving a second list of addresses associated with the at least one hardware resource, the second list of addresses listing backup operation information for the at least one hardware resource (col. 33 lines 7-40);

c) receiving a request to modify an operation of the at least one hardware resource in a given category (col. 33 lines 38-40);

d) modifying the second list of addresses to reflect the request to modify the operation of the at least one hardware resource (col. 33 lines 41-44);

e) exchanging the active/backup status of the first list of addresses and the second list of addresses (col. 33 lines 44-65);

f) duplicating the active second address list as replacement for the backup first list of addresses (col. 33 lines 44-65); and

g) operating the at least one hardware resource according to the modified active-status second list of addresses (col. 33 line 66 - col. 34 line 23).

14. As per claim 15, Kodosky teaches the invention as claimed, including in a communication device having a processor, a memory, and hardware resources all coupled to each other, a method of generating a scheduler for managing the hardware resources of the communication device, the method comprising the steps of:

a) receiving a quantity of available hardware resources (col. 30 line 66 - col. 31 line 25);

b) generating a list in the memory for linking requests to the hardware resources (col. 31 lines 45-49);

c) receiving a desired quantity of hardware resources to be operated on in the communication device (col. 31 lines 26-35);

d) receiving hardware resources operation information (col. 31 line 61 - col. 32 line 12);

e) receiving a request to use at least one of the hardware resources (col. 30 line 66 - col. 31 line 25; col. 46 lines 42-62);

f) assigning a memory address to the hardware resource operation information for each of the hardware resources (col. 33 lines 29-40); and

g) linking the memory addresses of hardware resources (col. 31 lines 36-37).

15. As per claim 16, Kodosky teaches the invention as claimed, including the method of claim 15, wherein the list is a table listing all virtual resources available for a given function (col. 31 lines 36-42).

16. As per claim 17, Kodosky teaches the invention as claimed, including the method of claim 15, wherein the list includes a primary table and a secondary table, the primary table tracking a group allocation and the secondary table mapping virtual uses (col. 32 lines 27-55; col. 33 lines 7-40).

17. As per claims 4 and 18-20, Kodosky teaches the invention as claimed, including an apparatus for performing the method of claims 3 and 15-17, respectively (Fig. 6).

Claim Rejections - 35 USC § 103

18. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

19. **Claims 1-2 and 5-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Prestifilippo et al. (USPN 5,446,889) (hereinafter Prestifilippo) in view of Kodosky.**

20. As per claim 1, Prestifilippo teaches the invention as claimed, including a method of controlling hardware resources in a device having a processor and a memory coupled to each other, the method comprising the steps of:

locating a first memory address in the memory associated with a first resource (col. 3 lines 9-10); and

determining a pointer that is associated with the first address and locates a subsequent address associated with a subsequent hardware resource (col. 3 lines 11-13).

21. Kodosky teaches the invention as claimed, wherein the information in the linked list is associated with a hardware resource (col. 31 lines 36-42); and

transmitting control information associated with the first memory address to the first hardware resource (col. 10 line 60 - col. 11 line 20).

22. It would have been obvious to one of ordinary skill in the art to combine Prestifilippo and Kodosky as Kodosky discusses the organizational structure of a linked list for storing operating information associated with hardware resources at length without discussion of a technique for traversing the list. Such traversal methods are largely well known in the art, but Prestifilippo teaches a method that is especially well suited for combination with Kodosky. Prestifilippo notes that linked lists can be used to store practically any kind of data, and the method of traversing linked lists disclosed by Prestifilippo is especially beneficial in the case of system crashes or hardware failures. In that sense, a well known organizational principle is applied to a programmable hardware system, such that the programmer can control the hardware implementation without fear of corruption of the underlying data structures.

23. As per claim 5, Prestifilippo teaches the invention as claimed, including in an electronic device having a processor, a memory, and hardware resources coupled to each other, a method of operating the hardware resources comprising the steps of:

a) locating a current address in the memory, the current address containing information associated with a current resource (col. 3 lines 9-10); and

c) reading a pointer, which is associated with the current address, that identifies a subsequent address containing subsequent information (col. 3 lines 11-13).

24. Kodosky teaches the invention as claimed, wherein the information in the linked list is associated with a hardware resource (col. 31 lines 36-42); and

b) transmitting operating information associated with the current address to the current hardware resource (col. 10 line 60 - col. 11 line 20).

25. As per claim 6, Kodosky teaches the invention as claimed, including the method of claim 5, wherein the method further comprises the step of:

d) determining whether the current hardware resource is reused within a system cycle (col. 31 lines 4-9, 29-35).

26. As per claim 7, Kodosky teaches the invention as claimed, including the method of claim 6, wherein if the current hardware resource is reused within a system cycle, further comprising the step of:

e) saving the current hardware resource information from a current use (col. 31 lines 58-61; col. 33 lines 50-65); and

f) repeating steps b), c), and d) until the current hardware resource is not reused within a system cycle (col. 33 lines 50-65).

27. As per claim 8, Kodosky teaches the invention as claimed, including the method of claim 6, wherein if the current hardware resource is not reused within a system cycle, further comprising the steps of:

e) determining whether operation should be terminated (col. 43 line 65 - col. 44 line 14); and

f) if operation should not be terminated, repeating steps a), b), c), and d) for a subsequent hardware resource that becomes the current hardware resource (col. 44 lines 15-24, 46-58).

28. As per claim 9, Kodosky does not specifically teach the invention as claimed, wherein the hardware resource is at least one of a searcher element, a downlink transmitter element, matched filter element, or tracker element. Rather, Kodosky discusses a system that is suited for controlling automation hardware, but is not limited to such an application (col. 12 lines 33-49). It would have been obvious to one of ordinary skill in the art that the method of Kodosky is applicable to a wide variety of implementations, providing hardware resources associated with a plethora of devices or applications.

29. As per claims 2 and 10-14, Kodosky teaches the invention as claimed, including an apparatus for performing the method of claims 1 and 5-9, respectively (Fig. 6).

Conclusion

30. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Syed J. Ali whose telephone number is (571) 272-3769. The examiner can normally be reached on Mon-Fri 8-5:30, 2nd Friday off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Meng-Ai T. An can be reached on (571) 272-3756. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Syed Ali
June 2, 2005

MENG-AI T. AN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 21